REMARKS

Claims 1-9 and 12-13 are pending in this application in which Claims 12-13 are withdrawn from further consideration. The Examiner rejected Claims 1-9 under 35 U.S.C. §112, first paragraph, and rejected Claims 1-9 under 35 U.S.C. §102(b). Claim 1 has been amended in the foregoing amendment.

Claim Rejections – 35 U.S.C. §112

Claims 1-9 were rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. In particular, the Examiner asserted that the phrase "common tangent plane" fails to exist within the specification. Claim 1 has been amended to define the invention by using the phrase "boundary surface" rather than "common tangent plane." Fig. 2 shows that the first and second semiconductor regions (14, 12) share a common boundary surface at the lower end surface of the first semiconductor region (14) and a portion of the upper end surface of the second semiconductor region (12). Accordingly, it is requested that this rejection be withdrawn.

Jambotkar Does Not Anticipate the Invention of Claims 1-9

Claims 1-9 were rejected under 35 U.S.C. 102(b) as anticipated by U.S. Patent No. 4,264,857 to Jambotkar ("*Jambotkar*"). This rejection is traversed for the reasons discussed below.

Claim 1

The Applicants amended Claim 1 to clarify that a second semiconductor region (12) of the first conductivity type is in contact with the lower end surface of the first semiconductor region (14) so as to share a common boundary surface by the first and second semiconductor regions. The semiconductor device of amended Claim 1 requires a first semiconductor region (14) of a first conductivity type, defined by an upper end surface, a lower end surface opposing to the upper end surface, and first and second side boundary

surfaces connecting the upper and lower end surfaces when viewed in section; a second semiconductor region (12) of the first conductivity type disposed under the first semiconductor region (14) and being in contact with the lower end surface of said first semiconductor region so as to share a common boundary surface by the first and second semiconductor regions; a third semiconductor region (13) of a second conductivity type disposed on the first semiconductor region (14) and being in contact with the upper end surface of said first semiconductor region (14); and a fourth semiconductor region (15) having first and second inner surfaces in contact with the first and second side boundary surfaces respectively when viewed in section and an impurity concentration lower than said first semiconductor region, configured such that the fourth semiconductor region is disposed between the second and third semiconductor regions (12, 13).

The Examiner contended that *Jambotkar* teaches a device comprising a first semiconductor region of a first conductivity type, defined by an upper end surface and a side boundary surface connecting the upper and lower end surfaces when viewed in section (Fig. 2A (16)); a second semiconductor region of the first conductivity type in metallurgical contact (s1) with the first semiconductor region at the lower end surface (Fig. 2A (14)); a third semiconductor region of a second conductivity type in metallurgical contact (B1) with the first semiconductor region at the upper end surface (Fig. 2A(12)); and a fourth semiconductor region having inner surface in metallurgical contact (W1) with the side boundary surface when viewed in section and an impurity concentration lower than the first semiconductor region, configured such that the fourth semiconductor region is disposed between the second and third semiconductor regions (Fig. 2A (10)).

Fig. 2A of *Jambotkar* illustrates semiconductor region 14 and semiconductor region 16. The accompanying text explains that one of the regions 14 is used as a source and the other region 16 is used as a drain of a field effect transistor. Column 2, lines 21-24. As shown in Figure 2A and as well-known in the art, the source and drain of a field effect

transistor are separate regions. Although a channel 20 connects the two regions 14, 16, the regions do not share a common boundary surface, as required by Claim 1. Similarly, the power supply terminals S1, D1 are connected to the regions, but do not provide a common boundary surface between the two regions.

Moreover, *Jambotkar* fails to describe a third semiconductor region of a second conductivity type disposed on the first semiconductor region and being in contact with the upper end surface of said first semiconductor region. The third semiconductor region 12 of *Jambotkar* is buried in the first semiconductor region 16, and thus the third and first semiconductor regions 12, 16 have a common top surface. Thus, the third semiconductor region 12 of *Jambotkar* cannot be disposed on the first semiconductor region 16 or be in contact with the upper end surface of the first semiconductor region 16.

Jambotkar also fails to describe a fourth semiconductor region having first and second inner surfaces in contact with the first and second side boundary surfaces respectively when viewed in section, configured such that the fourth semiconductor region is disposed between the second and third semiconductor regions. Even though the fourth semiconductor region 10 of *Jambotkar* is in contact with the bottom surface of the third semiconductor region 12, the inner surface of the fourth semiconductor region 10 does not contact with the side boundary surface of the first semiconductor region 16 due to the third semiconductor region 12 being inserted between the fourth semiconductor region 10 and the first semiconductor region 16. Furthermore, the fourth semiconductor region 10 of *Jambotkar* is not disposed between the second and third semiconductor regions 14, 12.

Accordingly, amended Claim 1 is not anticipated by *Jambotkar* and Claim 1 should be allowed.

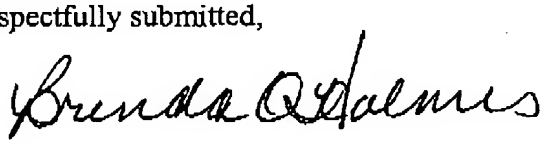
Claims 2-9

Claims 2-9 depend either directly or indirectly from amended Claim 1. The remarks made above in support of the patentability of independent Claim 1 are equally applicable in distinguishing dependent Claims 2-9 from *Jambotkar*. Accordingly, Claims 2-9 should also be allowed.

CONCLUSION

The foregoing is submitted as a complete response to the Office Action identified above. This application should now be in condition for allowance, and the Applicant solicits a notice to that effect. If there are any issues that can be addressed via telephone, the Examiner is asked to contact the undersigned at 404.685.6799.

Respectfully submitted,



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